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PHASE LOCKED LOOP BASED SOFT SWITCHING IMPLEMENTATION OF CLASS D SERIES RESONANT INVERTER

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ABSTRACT

Soft switching techniques are critical to minimize switching losses and improve system efficiency in power electronics systems. This study uses a CD4046 based phase locked loop (PLL) control system to optimize the zero current switching (ZCS) performance of a Class D series resonant inverter under dynamic load conditions. The system guarantees soft switching conditions by automatically monitoring the resonant frequency over a broad range of 27 kHz to 41 kHz. In the experimental study, the resonant frequency of the series resonant inverter is dynamically adjusted using a parallel connected capacitor bank, facilitating the assessment of the PLL system's adaptive performance. The results demonstrate that the system can effectively lock onto the resonant frequency, rapidly adapting to changes in load impedance while consistently maintaining zero current switching conditions.

1. INTRODUCTION

Power systems are important in converting, controlling, and distributing electrical energy. These systems overall performance and reliability depend mainly on the effectiveness of the switching techniques. Traditionally used hard switching methods cause high voltage and current surges during the turn on and turn off of power switches, resulting in significant switching losses [1]. These losses reduce system efficiency, create thermal stress on power switches, increase electromagnetic interference, and shorten the system's lifespan [2]. These issues become even more pronounced in high frequency applications. To address these adverse effects, extensive research has recently been conducted on soft switching techniques. Soft switching is a technique that minimizes switching losses by allowing power switches to operate at zero voltage or current. The main techniques for soft switching are zero voltage switching and zero current switching [3-4]. These techniques offer advantages over hard switching, including higher efficiency, lower thermal stress, and longer switch life [5-6]. Resonant converters, the backbone of power electronics circuits, store and transfer energy by exploiting the resonant properties of reactive elements like inductors and capacitors. Their diverse applications range from high frequency power supplies and DC motor drives to induction heating systems, wireless power transfer and LED lighting [7-8]. Integrating soft switching techniques with resonant converters significantly enhances these systems energy efficiency and performance [9-10]. However, to implement soft switching effectively, the switching instants must be precisely controlled according to the resonance conditions. Phase locked loop techniques provide an established mechanism to synchronize the switching instants with the resonant tank response, thereby improving robustness of soft switching operation under parameter and load variations [4,11-13]. PLL systems are feedback control circuits which lock the frequency and phase of an oscillator to a reference signal. They are essential in power system applications to automatically adjust the switching frequency of resonant converters to the resonant frequency and thus maintain soft switching conditions. This is critical to maintain system stability and efficiency, especially when load conditions or circuit parameters change. Recent studies have advanced resonant frequency tracking in different ways. Some works use resonant current estimation with PLL feedback [14]. Others rely on digitally implemented PLL structures for ultrasonic or resonant loads [15]. Measurement and

synchronization algorithms for dynamic resonant operation have also been reported [16]. Related approaches address load adaptation as the effective resonant point shifts [17]. These methods are effective. However, digital solutions often require additional sensing, computation, and firmware integration. This overhead may be undesirable in compact and low cost prototypes.

Despite extensive work on PLL assisted soft switching, low cost and fully analog implementations are still limited. This limitation is more apparent for CD4046 based solutions. Experimental studies that report quantitative tracking metrics under deliberate resonance shifts are scarce. To address this gap, this paper presents a CD4046 based analog PLL for a Class D series resonant inverter. The loop reduces the phase mismatch between the inverter output voltage and the load current. It locks the switching frequency to the tank resonance frequency. This behavior preserves ZCS during resonance variations. The system is experimentally validated by changing the tank parameters to shift the resonant frequency. The results report achieved ZCS conditions and frequency tracking accuracy. The proposed PLL controlled resonant inverter operates between 27 to 41 kHz and presents a good tracking performance.

2. MATERIAL AND METHOD

2.1. Series Resonant Inverter

Series resonant inverters use resonant circuits in which inductor and capacitor elements are connected in series to provide energy conversion in power electronics applications. These inverters are generally preferred in high frequency applications and aim to increase efficiency by operating at the resonance frequency [8]. The inductor and capacitor values in the circuit determine the resonance frequency and are expressed by Equation (1).

$$\omega_r = 2\pi f_r = \frac{1}{\sqrt{LC}} \tag{1}$$

Where f_r denotes the resonant frequency of the series RLC tank. L and C denote the resonant inductor and resonant capacitor, respectively. Class D series resonant inverters, unlike other series resonant converter topologies, connect the resonant capacitor to the negative terminal of the voltage source [18]. This connection simplifies the circuit design, making it more economical and user friendly. Figure 1(a) illustrates the basic circuit of a Class D series resonant inverter, and Figure 1(b) shows its equivalent circuit. In this inverter, two power switches are alternately turned on and off to apply a square wave voltage to the load.

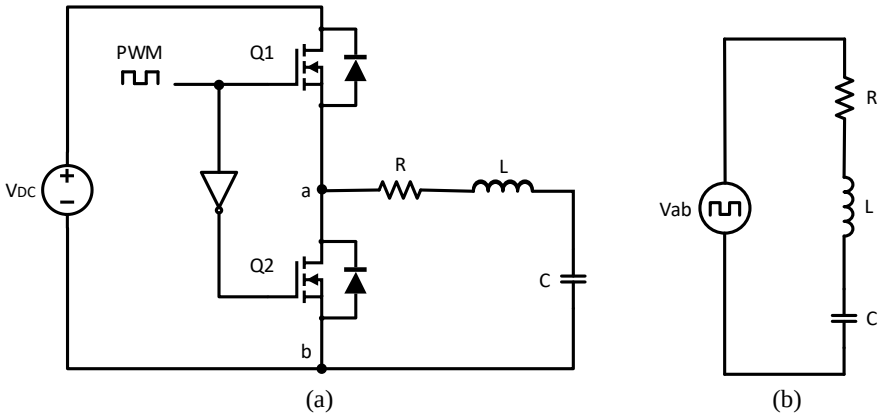


Figure 1. (a) Class D series resonant inverter; (b) Equivalent circuit.

The load impedance of this converter is defined by its resistance, inductive and capacitive reactance, as expressed in Equation (2).

$$Z = \sqrt{R^2 + \left(\omega L - \frac{1}{\omega C}\right)^2} \tag{2}$$

Where Z denotes the magnitude of the series RLC tank impedance. R represents the equivalent series resistance of the tank, including the load contribution. ω is the angular frequency. L and C denote the equivalent inductance and capacitance of the resonant tank, respectively. In Class D series resonant inverters, PLL systems are vital for determining the correct resonance frequency, minimizing the phase difference between current and voltage, and ensuring stable and soft switching conditions [13,19,20]. In this study, the Class D series resonant inverter is controlled by a pulse width modulated signal generator with a PLL circuit based on the CD4046 IC. This control loop prioritizes stability, allowing the converter to dynamically adjust to variations in load conditions while consistently remaining within the soft switching region.

2.2. Phase Locked Loop Design

A phase locked loop is a feedback control system designed to automatically synchronize the frequency and phase of an oscillator with a reference signal [21]. It consists of a phase comparator, a low pass filter, and a voltage controlled oscillator. The phase comparator identifies the phase difference between the reference signal and the signal generated by the voltage controlled oscillator (VCO), producing an error signal aimed at minimizing this difference. This error signal is then processed by the low pass filter and utilized to adjust the frequency of the VCO. The system iterates through this feedback loop until the frequency of the VCO aligns with that of the reference signal. Figure 2 presents the basic connection diagram of the CD4046 based PLL circuit, which illustrates the interconnection of the phase comparator, low pass filter, and VCO within the feedback loop.

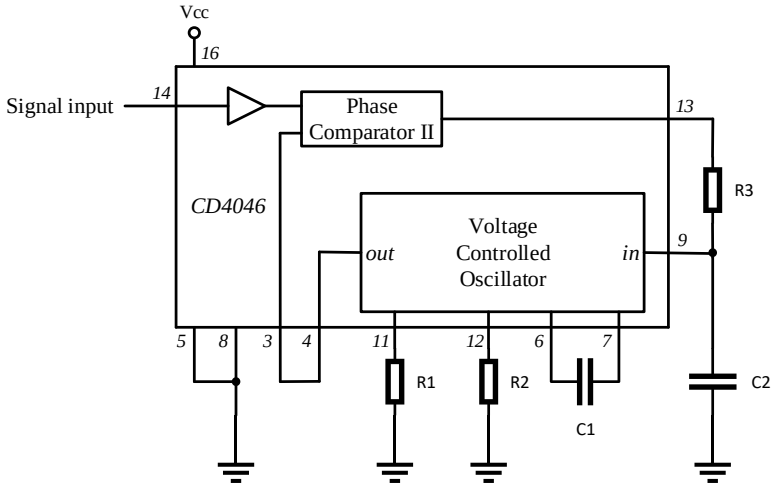


Figure 2. Basic connection of the CD4046 PLL circuit.

The VCO's frequency range depends on the externally connected R_1 and R_2 resistors and the C_1 capacitor [22]. Equations (3) and (4) express the minimum and maximum oscillator frequencies.

$$f_{min} = \frac{1}{R_2(C_1 + 32pF)} \tag{3}$$

$$f_{max} = f_{min} + \frac{1}{R_1(C_1 + 32pF)} \tag{4}$$

Where f_{min} and f_{max} denote the minimum and maximum free running frequencies of the CD4046 VCO. R_1 and R_2 are the external timing resistors and C_1 is the external timing capacitor that set the VCO frequency range [22]. A key parameter of PLL operation is the lock range, which defines the maximum frequency offset over which the loop remains locked once lock is achieved. For the CD4046 based design, the lock range is given by Equation (5).

$$2f_L = f_{max} - f_{min} \tag{5}$$

Where $2f_L$ denotes the PLL lock range, the frequency interval over which the loop sustains lock once acquired. The capture range characterizes the frequency interval over which the PLL can acquire lock from an unlocked condition. In the proposed implementation, the capture range f_c is primarily determined by the loop filter. Accordingly, for the first order low pass filter formed by R_3 and C_2, the capture range is approximated by Equation (6).

$$2f_c \approx \frac{1}{\pi}\sqrt{\frac{2\pi f_L}{R_3 C_2}} \tag{6}$$

2.3. System Design for PLL Controlled Class D Inverter

To establish the experimental test conditions, the minimum and maximum VCO frequency limits were set to 27 kHz and 41 kHz, respectively. In the experimental setup, C_1 was selected as 470 pF to obtain the targeted VCO frequency span. Subsequently, R_1 and R_2 were calculated as 78.8 kΩ and 152 kΩ using Equations (3) and (4).

A key design requirement is that the capture range given by Equation (6) must remain smaller than the lock range defined by Equation (5). Accordingly, the VCO timing network (R_1, R_2, C_1) was selected such that the free running frequency band between f_{min} and f_{max} covers the expected resonance variation of the inverter. This selection directly sets the available lock range expressed by $2f_L$ in Equation (5). The loop filter components (R_3, C_2) were then designed to ensure reliable acquisition under parameter variations, thereby determining the capture behavior described by Equation (6). In this study, the capture range was designed to be 6 kHz. Based on Equation (6), C_2 was chosen as 10 nF and R_3 was calculated as 3.1 kΩ, a standard value of 3.3 kΩ was used in the prototype. The resulting first order low pass filter processes the phase comparator error signal and applies the filtered control voltage to the VCO, which supports stable locking and frequency tracking over the intended operating interval.

2.4. Experimental Study

Minimizing switching losses in power electronic systems requires the effective application of soft switching techniques [18,23]. In practical implementations, their effectiveness depends on accurate synchronization of the switching instants with the resonant tank cycle. Accordingly, this study proposes an autonomous frequency tracking scheme that minimizes the phase shift between the inverter output voltage and the load current. The proposed control architecture employs a CD4046 based phase locked loop (PLL) to continuously adjust the switching frequency and maintain near resonant operation. Figure 3 presents the conceptual block diagram of the proposed CD4046 based PLL frequency tracking loop. Experimental validation is performed by implementing the hardware circuit in Figure 4 and measuring the inverter waveforms under intentionally shifted resonance conditions. In particular, the effective tank capacitance is adjusted to change the resonant frequency. The ability of the PLL to track this shift is verified using the measured oscilloscope waveforms and frequency readouts in Figure 5, together with the calculated to measured frequency comparison in Figure 6.

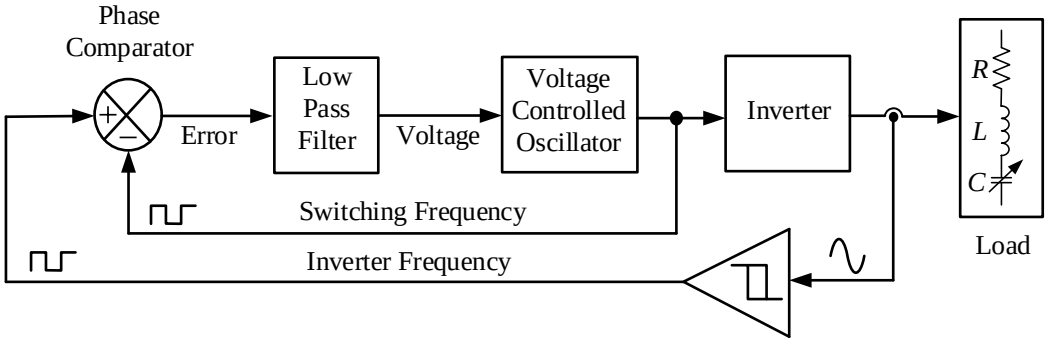
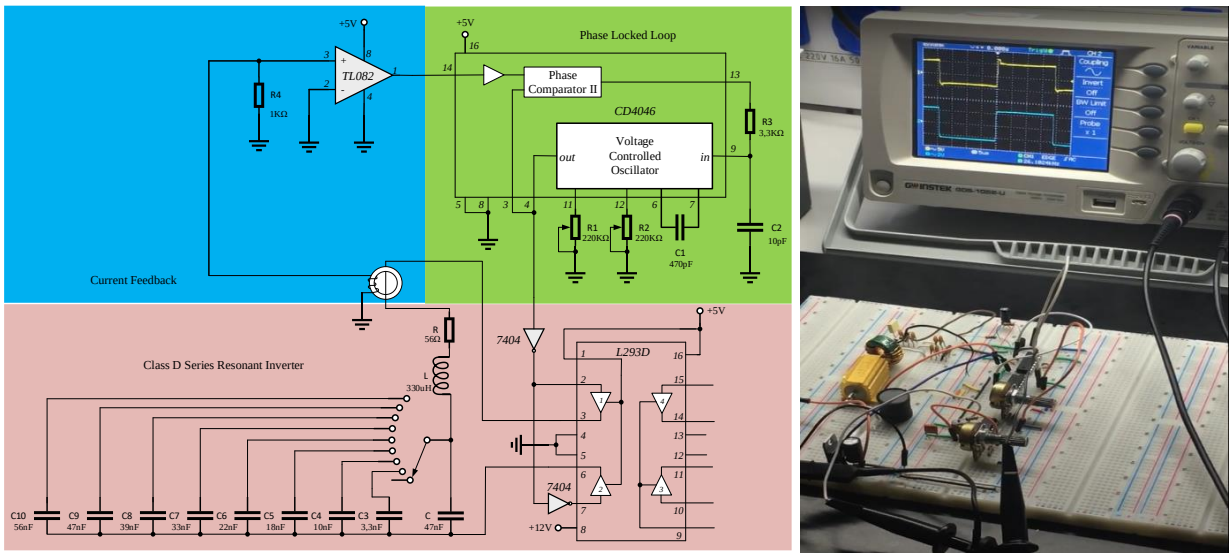


Figure 3. Block diagram of the proposed PLL controlled Class D series resonant inverter.

In the experimental setup, a Class D series resonant inverter is realized using the L293D driver integrated circuit and is driven by a PWM signal generated by a CD4046 based PLL [22]. The complete circuit schematic and the breadboard based implementation are provided in Figure 4(a) and Figure 4(b), respectively. The L293D is powered from a 12 V DC supply to drive the inverter stage [24].



(a) (b)

Figure 4. Experimental implementation of the proposed system: (a) Circuit schematic; (b) Breadboard based experimental setup (oscilloscope screen shows the conditioned square wave current feedback applied to the PLL).

The load current in the series resonant circuit was measured using a current transformer. Since the phase comparator of the CD4046 based PLL requires signals with the same waveform at its inputs, the sinusoidal inverter current cannot be applied directly to the PLL. Therefore, the measured inverter current was converted to a square wave using a zero crossing detector based on the TL082. The resulting square wave current signal was applied to the phase comparator input of the PLL and compared with the inverter's switching signal to generate a phase error signal. The square wave shown in the oscilloscope image in the prototype based experimental setup corresponds to the converted current signal used by the PLL. The sinusoidal wave in Figure 5 corresponds to the measured resonance current before the zero crossing conversion stage. This structure ensures that the PLL accurately tracks the resonance frequency and maintains stable ZCS under varying load conditions. In the experiments, the resonance frequency was intentionally varied by connecting different capacitor values in parallel with the 47 nF main capacitor, and the proposed system was evaluated under deliberately induced resonance shifts.

3. RESULTS AND DISCUSSION

The soft switching performance of the CD4046 based PLL controlled Class D series resonant inverter was experimentally evaluated under capacitance induced resonance shifts. The measurements show that the PLL dynamically tracks the resonant point and updates the switching frequency accordingly. The waveforms displayed on the oscilloscope in Figure 5 show the inverter output voltage on CH_1 (5 V/div) and the RLC load current, measured via a current transformer, on CH_2 (400 mV/div). The measurements were taken with a time base setting of 10 microseconds/div. For all tested effective capacitance values, the switching instants remain aligned with the load current zero crossings, confirming that zero current switching (ZCS) is maintained during resonance transitions. Following each capacitance change, only a short transient is observed and the loop relocks rapidly at the new operating condition, indicating stable tracking under time varying tank parameters.

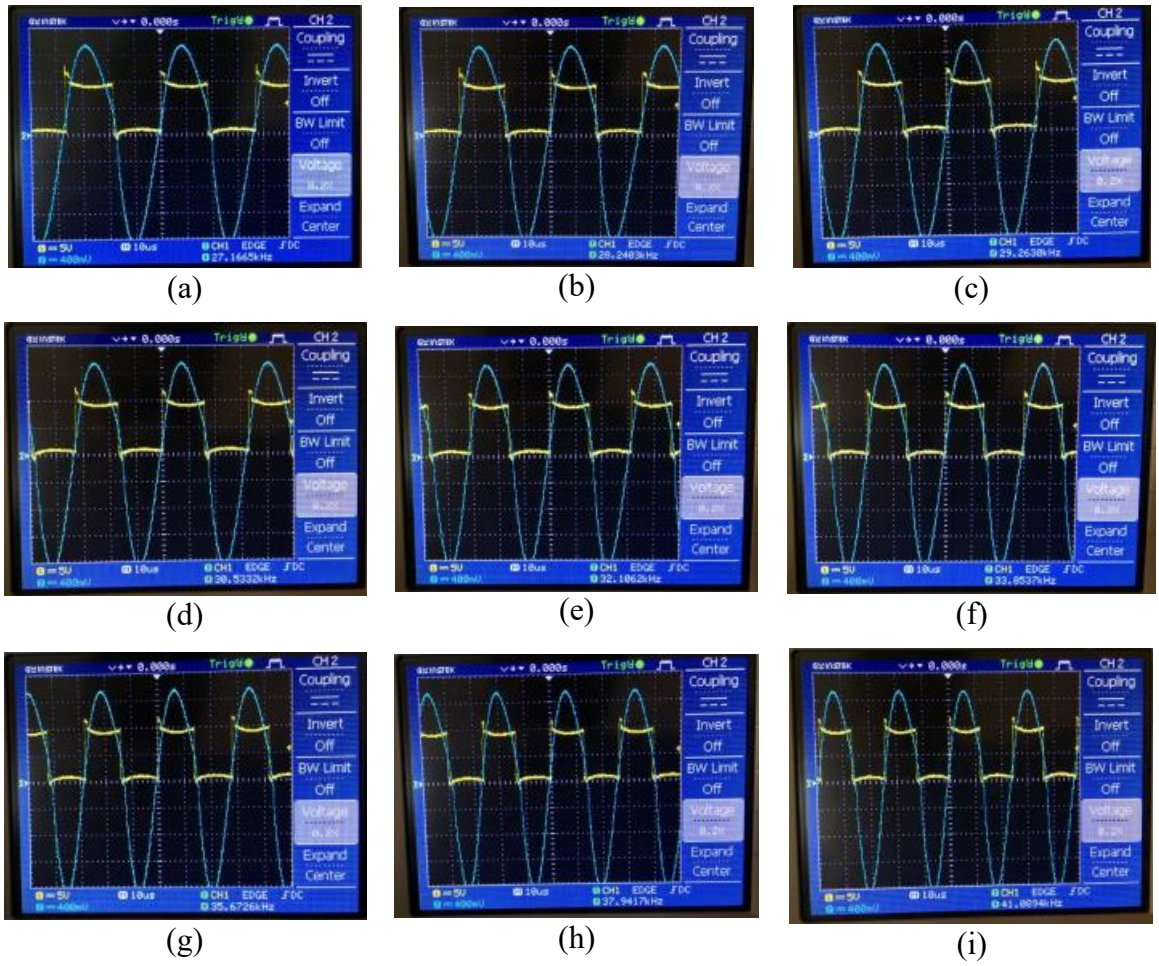


Figure 5. Measured output voltage (CH_1) and RLC load current (CH_2) waveforms under capacitance induced resonance shifts. (a)-(i) correspond to effective tank capacitances of 103, 94, 86, 80, 69, 65, 57, 50.3, and 47 nF respectively.

Figure 6 illustrates the performance of PLL control, showing the convergence behavior of the switching frequency measured under different operating conditions to the calculated resonance frequency. Notably, the PLL circuit adaptively adjusts the switching frequency in response to changes in the resonance frequency caused by the inclusion or exclusion of capacitor bank elements. This adaptive behavior clearly indicates the system's stability, reassuring the users about its reliability within a 14 kHz operating range.

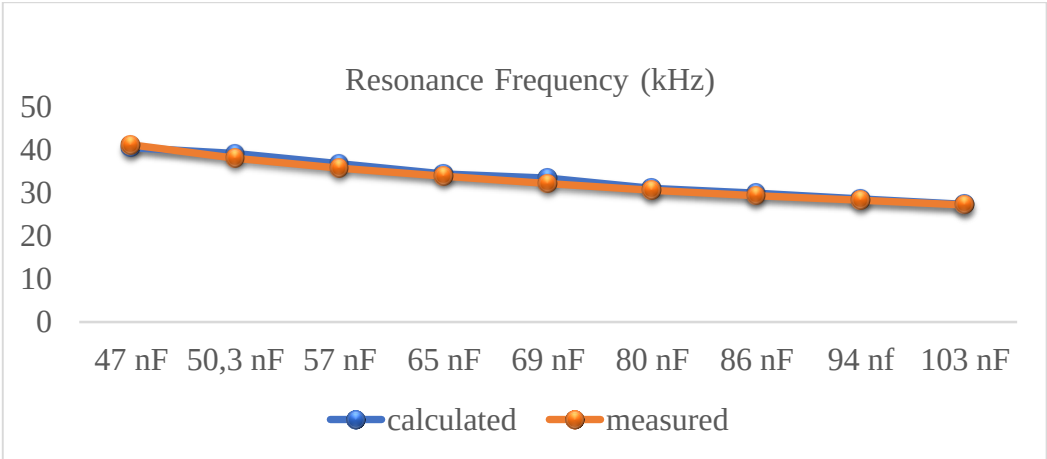


Figure 6. Comparison of the calculated resonant frequency and the measured PLL switching frequency versus effective tank capacitance.

The results in Table 1 quantitatively demonstrate the frequency tracking accuracy of the proposed CD4046 based analog PLL.

Table 1. Comparison of calculated resonant frequency and measured PLL locked switching frequency under different capacitance values (L = 330 µH, R = 56 Ω).

Case	$C_{eq.}$ (nF)	f_r (kHz)	f_s (kHz)	Error (kHz)	Error (%)
(a)	103	27.3	27.1	0.2	0.6
(b)	94	28.6	29.2	-0.7	-2.3
(c)	86	29.9	29.3	0.6	2.0
(d)	80	31.0	30.5	0.4	1.4
(e)	69	33.4	32.2	1.2	3.6
(f)	65	34.4	33.7	0.7	2.1
(g)	57	36.7	35.7	1.0	2.8
(h)	50.3	39.1	37.9	1.1	2.9
(i)	47	40.4	41.0	-0.6	-1.5

Throughout the capacitance range examined, the measured switching frequency closely follows the calculated resonance frequency, with a maximum deviation of 1.2 kHz and a percentage error of 3.6%. This level of agreement confirms that the PLL maintains effective synchronization with the resonant tank despite significant parameter variations. Therefore, the proposed low cost analog control structure achieves robust dynamic tracking performance without requiring a digital controller. Since the primary focus of this study is the experimental validation of dynamic resonance tracking rather than efficiency optimization, a detailed numerical efficiency analysis is not included. However, accurate frequency tracking and sustained zero current switching, as evidenced by the results in Table 1 and the measured waveforms, inherently contribute to reduced switching losses. A comprehensive efficiency evaluation, including detailed power loss measurements, is identified as a subject of future work.

4. CONCLUSION AND SUGGESTIONS

A CD4046 based PLL control system has been developed and experimentally tested to optimize the soft switching performance of D class series resonant converters under resonance shifts. The developed system successfully maintained ZCS conditions over a wide frequency range of 27 to 41 kHz and quickly adapted to changes in load. Minor discrepancies between theoretical and experimental results have been attributed to the tolerances of passive components. Nevertheless, the PLL control system has been confirmed to be robust against these variations. This indicates that the proposed system can operate reliably in applications with variable or unpredictable load profiles.

Conflict of Interest Statement

There is no conflict of interest between the authors.

Statement of Research and Publication Ethics

The study is complied with research and publication ethics.

Artificial Intelligence (AI) Contribution Statement

This manuscript was entirely written, edited, analyzed, and prepared without the assistance of any artificial intelligence (AI) tools. All content, including text, data analysis, and figures, was solely generated by the authors.

Contributions of the Authors

Kadir Eker: Conceptualization, Methodology, Hardware Implementation, Investigation, Data Curation, Formal Analysis, Writing Original Draft Preparation, Visualization.

Selim Öncü: Supervision, Writing Review and Editing, Resources.

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